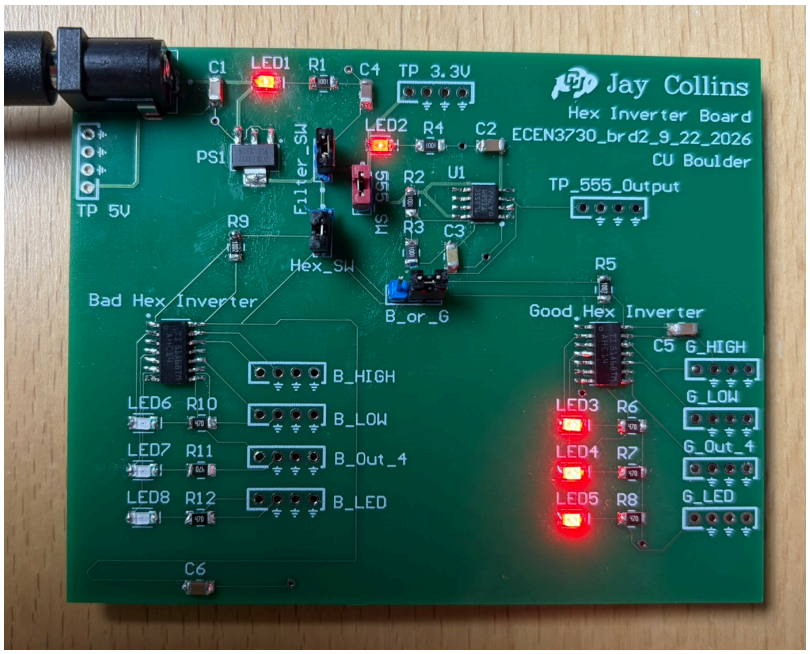
ECEN 3730: Board 2 Report

Hex Inverter Noise Circuit



Jay Collins

Description:

This board has two identical hex inverter circuits driven by a 555 timer, one with good layout practices and one with bad, to compare their switching noise.

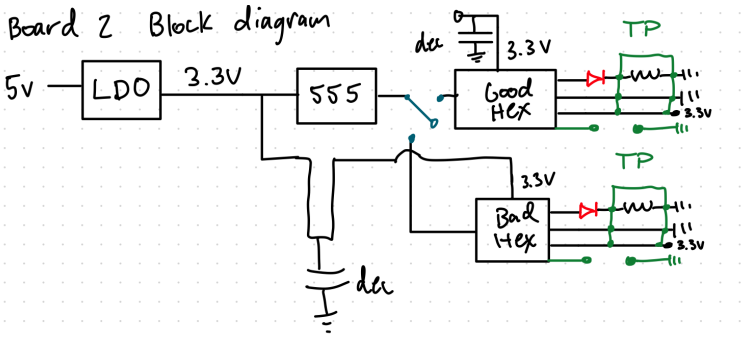
Plan of Record:

The circuit board will contain:

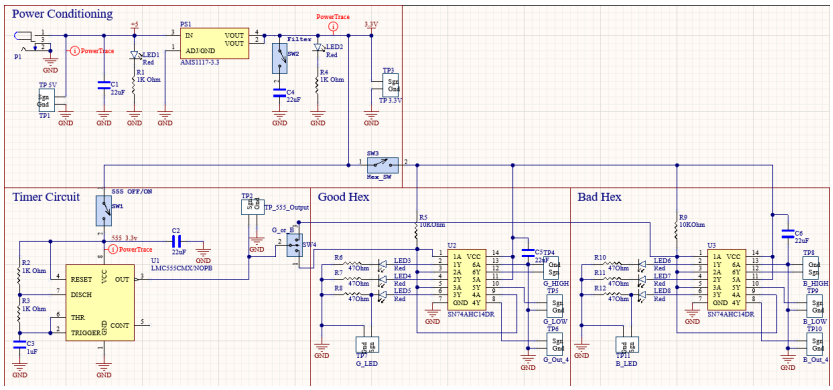
1. A power plug for an external 5V AC to DC charger, and an AMS1117 LDO that drops the 5V rail to 3.3V for the hex inverters.
2. A 555 timer chip (LMC555) and circuitry designed for about 500 Hz and 60% duty cycle.
3. Two identical hex inverter (74AHC14) circuits; one with a close decoupling capacitor and a ground plane underneath, and one with a far capacitor with no ground plane underneath
4. A dedicated 3-pin switch to connect the 555 output to either the good or bad layout
5. Indicator lights, test points and isolation switches as appropriate
6. Four of the six inverters in each hex package are driven: three outputs drive LED and 50Ω loads, and the fourth goes to a test point as the scope trigger. The remaining two are set up as a quiet high and a quiet low. All parts are 1206.

Datasheets: LMC555, AMS1117, 74AHC14

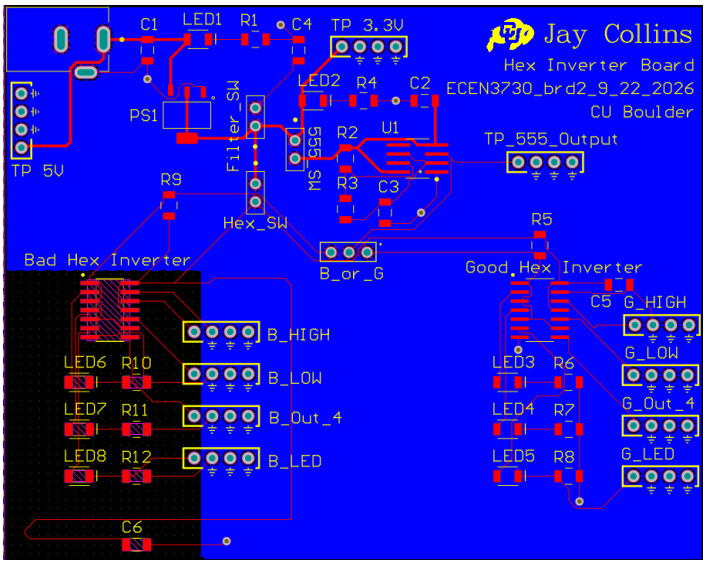
Block Diagram:



Schematic:



Layout:



Requirements to “work”:

- When powered with the 5V charger, all the LEDs turn on, including the power rail and 3.3V indicators, and the LDO outputs 3.3V.
- The 555 timer generates a square wave signal with a frequency and duty cycle of about 500 Hz and 60% duty cycle.
- The switches control the 555 timer, the hex inverters, and which inverter receives the 555 output signal.
- When measuring the outputs of the hex inverters, one of them should have minimal switching noise while the other has much more noticeable noise.
- The quiet high should measure at around 3.3V and the quiet low should be 0V, the out LEDs should all be on, and from the LED-free out, there should be a square wave.

Schedule, Risks and Testing Plans:

Schedule:

- 9/22 layout complete, 9/23 CDR and board submission, 10/12 assembly and measurements, 10/23 report due.

Risks:

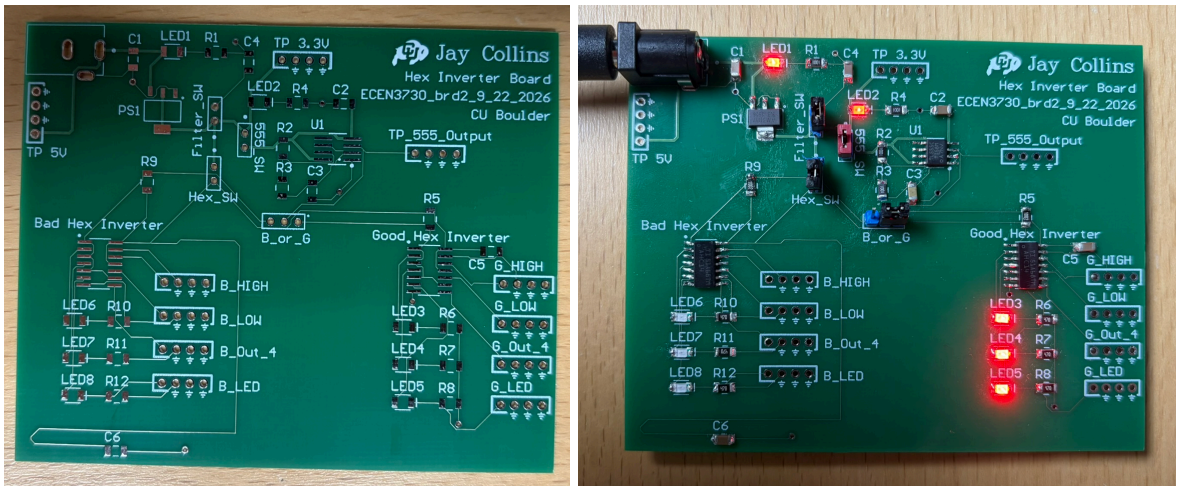
- Wrong parts or incorrect connections. To avoid this, I double checked the parts, and multiple people as well as the TA verified the schematic.
- Poor soldering. I will follow good soldering practices to mitigate this risk.

Testing plans:

- The main measurement on this board will be comparing the switching noise on the quiet high and low outputs on the good and bad circuits. To do this, I will connect two scope probes at a time, one to the trigger test points, and one on either the quiet high or quiet low outputs.
- I will also capture the LED current and calculate the hex inverter Thevenin resistance, seeing if they differ at all between the bad and good circuits.
- To verify expected voltage rail values, I will also test both the 5V input as well as the LDO 3.3V output.

Implementation:

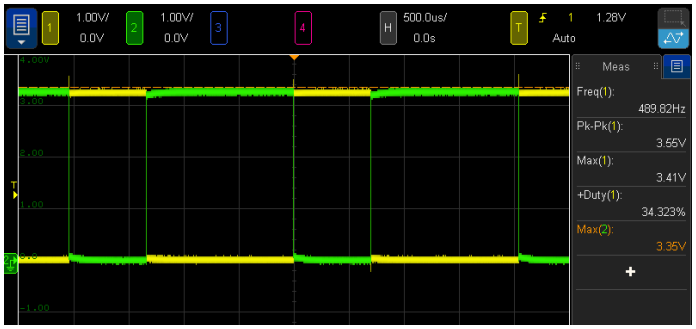
Upon the first plug in, the board turned on and all of the connected LEDs turned on. The correct functionality was verified by testing the power rails, the 555 timer output, and the output of both of the hex inverters. Both the power indicator LEDs turned on and the measured outputs were 5.2V and 3.31V for each rail. Up next, I will be going through the differences between the good and bad layouts.



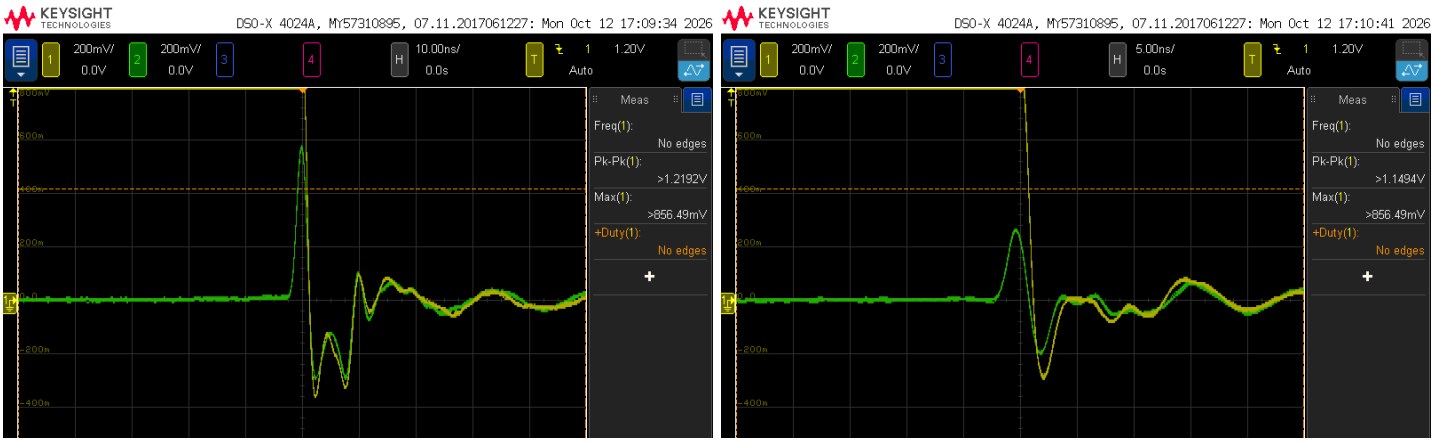
Nonassembled vs Assembled

Scope Measurements and Calculations:

The first measurement is the 555 timer output with the good hex inverter probed at the same time. The duty cycle is roughly 60%, the frequency is about 500 Hz, and the peak voltage is about 5V. The 555 timer is outputting what is expected and the hex inverter is operating correctly.

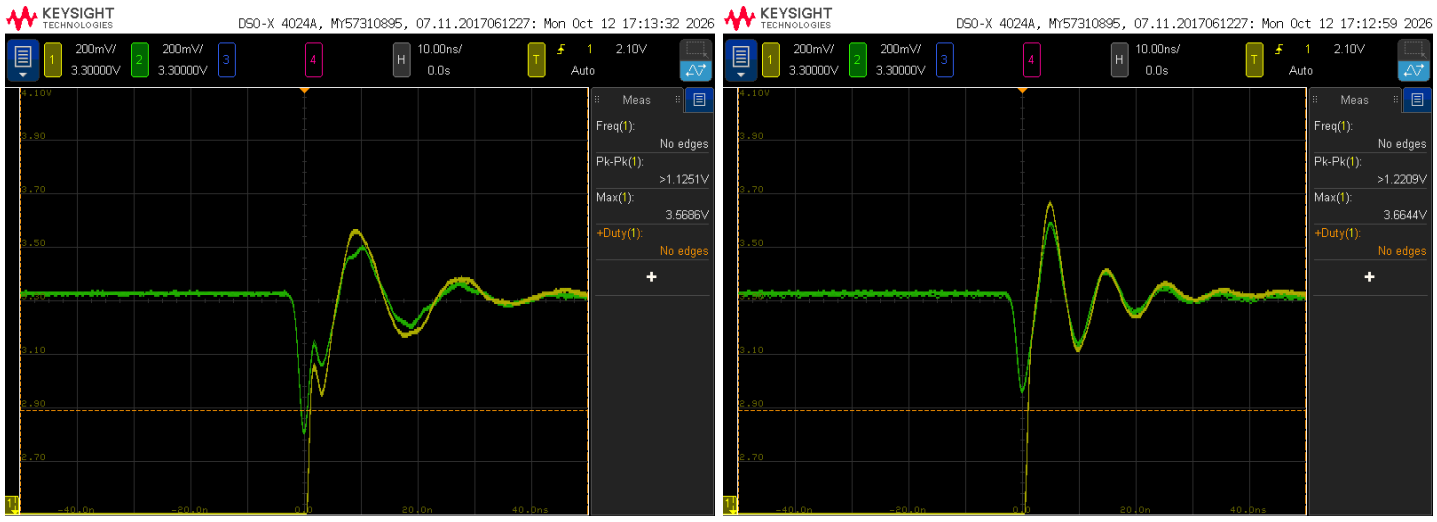


The next measurements are going to be comparing the switching noise on the falling edge from the quiet low pin on both the bad and good hex inverter setups.



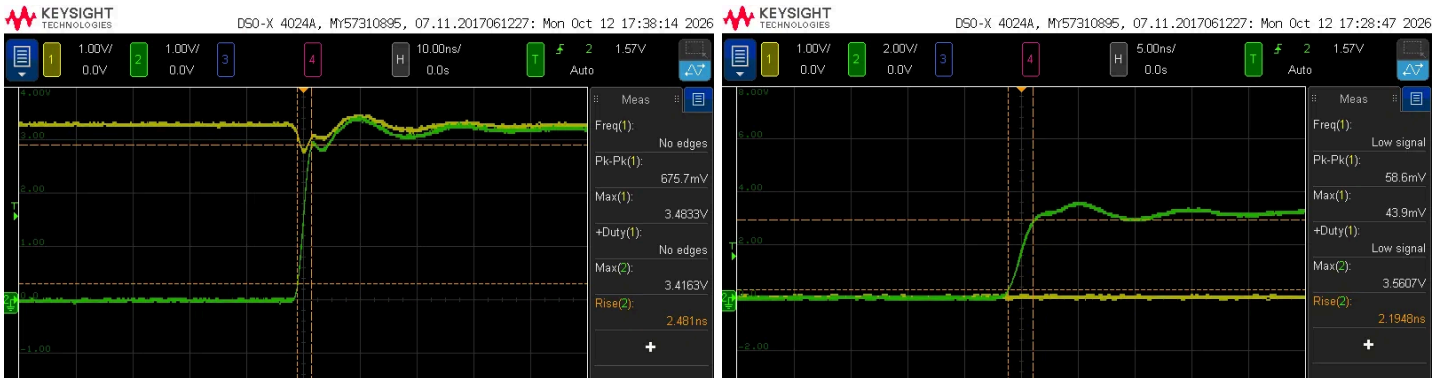
No Ground Plane vs With Ground Plane

On the side without a ground plane, the quiet low fluctuated about 900mV initially upon the switching of the other hex inverter pins. On the side with the ground plane, it was closer to just 500mV. This shows that having a ground plane reduces noise because the return current can take a low-inductance path directly under the signal, which reduces the L·dI/dt ground bounce. Up next, I will show the differences on the rising edge between the two quiet high outputs.



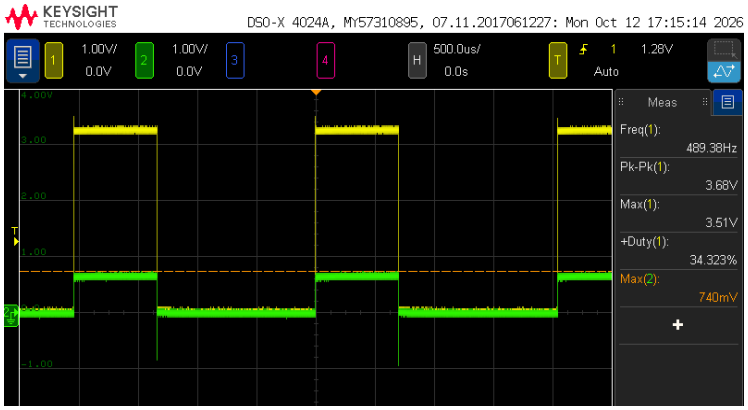
Far Capacitor vs Close Capacitor

As shown above, the bad layout droops further down than the good layout and has a larger peak-to-peak on the noise, about 800mV vs 720mV. Both sides use a 22uF capacitor. The changes are not drastic but it is enough to affect a higher frequency signal. In the future, I will make sure to place decoupling capacitors as close as physically possible to the point they are decoupling. Next, I will compare the risetime on either side, shown below.



Bad Layout vs Good Layout

The risetimes are very similar, with the good layout being about 0.3ns faster. The slower risetime on the bad layout could also contribute to the switching noise not looking that bad, because the L·dI/dt voltage is smaller when the current changes more slowly. Finally, I will be calculating the Thevenin resistance of the hex inverter. I will show this by measuring the current through one of the LEDs, with that measurement being shown below.



The voltage across each 50Ω resistor peaked at 740mV on both the good and bad layouts, so each loaded output is sourcing 0.74V/50Ω = 14.8mA, or about 44.4mA total with all three outputs switching. Since I did not capture the loaded output pin voltage, I estimated the LED drop at about 2.0V, a typical value for an indicator LED, which puts the loaded pin at about 2.74V, 0.56V below the unloaded 3.3V. The Thevenin resistance of the hex inverter output is then 0.56V/14.8mA = 38Ω, and since the current was identical on both layouts, this estimate applies to both.

Here is a Summary table.

Bad Layout	**Good Layout**
900mV fluctuation on quiet low	500mV fluctuation on quiet low
800mV fluctuation on quiet high	720mV fluctuation on quiet high
2.5ns risetime	2.2ns

Project Analysis:

Practices that worked well:

- Labeling the individual components on the board made it easy to assemble.
- Using 10x probes for the test points along with a ground spring.
- Having a ground plane proved to be better (quiet low noise fell from 900mV to 500mV).
- Placing the decoupling capacitor close to the IC gave less droop and less peak-to-peak noise on the quiet high (720mV vs 800mV), a smaller effect than the ground plane had on the quiet low.

- The use of indicator LEDs, test points, and switches made it very easy to obtain accurate measurements.

What I would have done differently:

- I should have taken all measurements on the same edge instead of switching between rising and falling.
- I should have measured the voltage at the inverter pin for the voltage drop to get a real number instead of an estimate.
- I should have captured the rail noise and compared it vs quiet high.

No hard errors occurred and the board worked on the first power-up. One shortfall was that the quiet high noise differed by only 80mV between the layouts (800mV vs 720mV), less of a difference than the much more noticeable noise I set as a requirement.

Conclusion:

This project truly demonstrated why it is important to follow good design practices when I create PCBs. Giving signals a clean, short path to the ground plane as well as properly placed decoupling capacitors are very important as expected. Taking real measurements showed exactly how the signals were affected. Even though the schematic was the same for both circuits, the layout was different, emphasizing that when creating the layout from the schematic, simply wiring up all the components however I want is not going to be good enough. I need to take into consideration what components need to physically be closer or further away from each other to maintain signal integrity. In the future, I will do exactly that. Recommendations: keep a continuous ground plane under every IC and place each decoupling capacitor next to its power pin with a short ground connection.